AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. **(Currently amended)** A method of operating an integrated circuit having a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said modifiable conductance switch devices comprising thin film transistor (TFT) devices, said method comprising pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block.

2. (Original) The method of claim 1 further comprising performing a read operation only after at least two programming pulses.

3. (Original) The method of claim 1 further comprising maintaining an inhibit voltage on associated array lines between programming pulses.

4. (Original) The method of claim 1 wherein the leakage current effects include changes in a voltage bias at one or more locations within a NAND string that otherwise may occur during a long programming pulse.

5. (Original) The method of claim 4 further comprising re-establishing a respective bias condition within selected and unselected NAND strings of a selected block before each such programming pulse.

6. **(Currently amended)** ~~The method of claim 1 further comprising:~~ A method of operating an integrated circuit having a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said method comprising:

pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block;

coupling unselected NAND strings within a selected memory block to associated array lines conveying an inhibit voltage; and

de-coupling unselected NAND strings within the selected memory block from other associated array lines conveying bias voltages other than the inhibit voltage. [[;]]

7. (Original) The method of claim 6 further comprising maintaining the inhibit voltage on the associated array lines between programming pulses.

8. (Original) The method of claim 6 further comprising:

driving the selected word line to a voltage less than the programming voltage while unselected NAND strings are coupled to the associated array lines conveying the inhibit voltage; then

decoupling the unselected NAND strings from the associated array lines conveying the inhibit voltage; and

pulsing the selected word line to the programming voltage.

9. (Original) The method of claim 8 wherein:

the selected word line is brought to ground before decoupling unselected NAND strings from the associated array lines conveying the inhibit voltage, and then driven to the programming voltage.

10. (Original) The method of claim 6 wherein the de-coupling unselected NAND strings step comprises turning off at least one of a plurality of series select devices at an end of the selected NAND strings.

11. (Original) The method of claim 10 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

12. (Original) The method of claim 1 further comprising:

coupling the selected NAND string to an associated array line conveying one of either a bit line programming voltage to program the selected memory cell or a bit line inhibit voltage to inhibit programming of the selected memory cell; and

de-coupling the selected NAND string from other associated array lines.

13. (Original) The method of claim 12 wherein the de-coupling the selected NAND string step comprises turning off at least one of a plurality of series select devices at an end of the selected NAND strings.

14. (Original) The method of claim 13 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

15. (Original) The method of claim 13 wherein the turning off step comprises driving to different levels respective select signals corresponding to at least two respective ones of the plurality of series select devices at the end of the selected NAND string.

16. (Original) The method of claim 15 wherein one of the different levels is ground, and another of the different levels is a voltage between ground and a programming voltage conveyed on a selected word line.

17. **(Currently amended)** ~~The method of claim 1~~ A method of operating an integrated circuit having a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said method comprising:

pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block;

wherein individual programming pulses are shorter than one microsecond, and the aggregate programming time is longer than ten microseconds.

18. **(Currently amended)** ~~The method of claim 1~~ A method of operating an integrated circuit having a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said method comprising:

pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block;

wherein the programming voltage is within the range from 10 to 16 volts.

19. **(Currently amended)** The method of claim 6 ~~claim 1~~ wherein the memory array comprises a two-dimensional memory array having one plane of memory cells formed in a substrate.

20. (Original) The method of claim 1 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

21. (Original) The method of claim 20 further comprising performing a read operation only after at least two programming pulses.

22. (Original) The method of claim 20 further comprising maintaining an inhibit voltage on associated array lines between programming pulses.

23. (Original) The method of claim 20 further comprising re-establishing a respective bias condition within selected and unselected NAND strings of a selected block before each such programming pulse.

24. **(Currently amended)** The method of claim 20 further comprising:

coupling unselected NAND strings within a selected memory block to associated array lines conveying an inhibit voltage; and

de-coupling unselected NAND strings within the selected memory block from <u>other</u> associated array lines conveying bias voltages other than the inhibit voltage<u>.</u> [[;]]

25. (Original) The method of claim 24 further comprising maintaining the inhibit voltage on the associated array lines between programming pulses.

26. (Original) The method of claim 24 further comprising:

driving the selected word line to a voltage less than the programming voltage while unselected NAND strings are coupled to the associated array lines conveying the inhibit voltage; then

decoupling the unselected NAND strings from the associated array lines conveying the inhibit voltage; and

pulsing the selected word line to the programming voltage.

27. (Original) The method of claim 26 wherein:

the selected word line is brought to ground before decoupling unselected NAND strings from the associated array lines conveying the inhibit voltage, and then driven to the programming voltage.

28. (Original) The method of claim 24 wherein the de-coupling unselected NAND strings step comprises turning off at least one of a plurality of series select devices at an end of the selected NAND strings.

29. (Original) The method of claim 28 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

30. (Original) The method of claim 20 further comprising:

coupling the selected NAND string to an associated array line conveying one of either a bit line programming voltage to program the selected memory cell or a bit line inhibit voltage to inhibit programming of the selected memory cell; and

de-coupling the selected NAND string from other associated array lines.

31. (Original) The method of claim 30 wherein the de-coupling the selected NAND string step comprises turning off at least one of a plurality of series select devices at an end of the selected NAND strings.

32. (Original) The method of claim 31 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

33. (Original) The method of claim 31 wherein the turning off step comprises driving to different levels respective select signals corresponding to at least two respective ones of the plurality of series select devices at the end of the selected NAND string.

34. (Original) The method of claim 33 wherein one of the different levels is ground, and another of the different levels is a voltage between ground and a programming voltage conveyed on a selected word line.

35. (Original) The method of claim 20 wherein individual programming pulses are shorter than one microsecond, and the aggregate programming time is longer than ten microseconds.

36. (Original) The method of claim 20 wherein the programming voltage is within the range from 10 to 16 volts.

37. (Original) The method of claim 20 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

38. (Original) The method of claim 37 wherein NAND strings of a given memory plane include selection devices formed above the substrate.

39. (Original) The method of claim 1 wherein the modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage at least some of the time.

40. (Original) The method of claim 1 wherein the modifiable conductance switch devices comprise devices chosen from the group consisting of:

a device including a floating gate electrode;

a device including silicon nanoparticles;

a device including a polarizable material; and

a device including a ferroelectric material.

41. **(Currently amended)** The method of claim 6 ~~claim 1~~ wherein the modifiable conductance switch devices comprise thin film transistor (TFT) devices.

42. **(Currently amended)** The method of claim 1 wherein the ~~memory cell~~ modifiable conductance switch devices have more than two nominal values of conductance, for storing more than one bit of data per memory cell.

43. **(Currently amended)** ~~The method of claim 1~~ A method of operating an integrated circuit having a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said method comprising:

pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block;

wherein the modifiable conductance switch devices comprise transistors having a charge storage dielectric.

44. (Original) The method of claim 43 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

45. **(Currently amended)** The method of claim 43 wherein the ~~memory cell~~ transistors have a depletion mode threshold voltage for at least one of two data states.

46. **(Currently amended)** An integrated circuit comprising:

a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices, said modifiable conductance switch devices comprising thin film transistor (TFT) devices;

array support circuitry configured for pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block.

47. (Original) The integrated circuit of claim 46 wherein the array support circuitry is further configured for performing a read operation only after at least two programming pulses.

48. (Original) The integrated circuit of claim 46 wherein the array support circuitry is further configured for maintaining an inhibit voltage on associated array lines between programming pulses.

49. (Original) The integrated circuit of claim 46 wherein the leakage current effects include changes in a voltage bias at one or more locations within a NAND string that otherwise may occur during a long programming pulse.

50. (Original) The integrated circuit of claim 49 wherein the array support circuitry is further configured for re-establishing a respective bias condition within selected and unselected NAND strings of a selected block before each such programming pulse.

51. **(Currently amended)** ~~The integrated circuit of claim 46 further comprising~~ An integrated circuit comprising:

a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices;

array support circuitry configured for pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block; and

means for coupling unselected NAND strings within a selected memory block to associated array lines conveying an inhibit voltage to establish a bias condition within such unselected NAND strings.

52. (Original) The integrated circuit of claim 51 wherein the array support circuitry is further configured for maintaining the inhibit voltage on the associated array lines between programming pulses.

53. (Original) The integrated circuit of claim 51 further comprising:

means for driving the selected word line to a voltage less than the programming voltage while unselected NAND strings are coupled to the associated array lines conveying the inhibit voltage;

means for then decoupling, before the selected word line programming pulse, the unselected NAND strings from the associated array lines conveying the inhibit voltage.

54. (Original) The integrated circuit of claim 51 comprising a respective plurality of series select devices at an end of each NAND string.

55. (Original) The integrated circuit of claim 51 further comprising means for turning off at least one of a plurality of series select devices at an end of the selected NAND strings.

56. (Original) The integrated circuit of claim 54 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

57. (Original) The integrated circuit of claim 46 further comprising means for coupling the selected NAND string to an associated array line conveying one of either a bit line programming voltage to program the selected memory cell or a bit line inhibit voltage to inhibit programming of the selected memory cell.

58. (Original) The integrated circuit of claim 57 further comprising means for turning off at least one of a plurality of series select devices at an end of the selected NAND strings.

59. (Original) The integrated circuit of claim 58 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

60. (Original) The integrated circuit of claim 58 wherein the respective select signals corresponding to at least two respective ones of the plurality of series select devices at the end of the selected NAND string are driven to different levels.

61. (Original) The integrated circuit of claim 60 wherein one of the different levels is ground, and another of the different levels is a voltage between ground and a programming voltage conveyed on a selected word line.

62. **(Currently amended)** ~~The integrated circuit of claim 46~~ <u>An integrated circuit comprising:</u>

<u>a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices;</u>

<u>array support circuitry configured for pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block,</u> wherein individual programming pulses are shorter than one microsecond, and the aggregate programming time is longer than ten microseconds.

63. **(Currently amended)** ~~The integrated circuit of claim 46~~ An integrated circuit comprising:

a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices;

array support circuitry configured for pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block, wherein the programming voltage is within the range from 10 to 16 volts.

64. **(Currently amended)** The integrated circuit of claim 51 ~~claim 46~~ wherein the memory array comprises a two-dimensional memory array having one plane of memory cells formed in a substrate.

65. (Original) The integrated circuit of claim 46 wherein the memory array comprises a three-dimensional memory array having at least two planes of memory cells formed above a substrate.

66. (Original) The integrated circuit of claim 65 further comprising:

means for performing a read operation only after at least two programming pulses; and

means for maintaining an inhibit voltage on associated array lines between programming pulses.

67. (Original) The integrated circuit of claim 65 further comprising means for re-establishing a respective bias condition within selected and unselected NAND strings of a selected block before each such programming pulse.

68. **(Currently amended)** The integrated circuit of claim 65 further comprising:

means for coupling unselected NAND strings within a selected memory block to associated array lines conveying an inhibit voltage; and

means for de-coupling unselected NAND strings within the selected memory block from other associated array lines conveying bias voltages other than the inhibit voltage. [[;]]

69. (Original) The integrated circuit of claim 68 further comprising means for maintaining the inhibit voltage on the associated array lines between programming pulses.

70. (Original) The integrated circuit of claim 68 further comprising:

means for driving the selected word line to a voltage less than the programming voltage while unselected NAND strings are coupled to the associated array lines conveying the inhibit voltage;

means for then decoupling, before the selected word line programming pulse, the unselected NAND strings from the associated array lines conveying the inhibit voltage.

71. (Original) The integrated circuit of claim 68 comprising a plurality of series select devices at an end of each NAND string.

72. (Original) The integrated circuit of claim 71 wherein the respective plurality of select devices and memory cell devices forming each NAND string are structurally substantially identical.

73. (Original) The integrated circuit of claim 65 further comprising:

means for coupling the selected NAND string to an associated array line conveying one of either a bit line programming voltage to program the selected memory cell or a bit line inhibit voltage to inhibit programming of the selected memory cell.

74. (Original) The integrated circuit of claim 65 further comprising means for driving to different levels respective select signals corresponding to at least two respective ones of a plurality of series select devices at the end of the selected NAND string.

75. (Original) The integrated circuit of claim 74 wherein one of the different levels is ground, and another of the different levels is a voltage between ground and a programming voltage conveyed on a selected word line.

76. (Original) The integrated circuit of claim 65 wherein individual programming pulses are shorter than one microsecond, and the aggregate programming time is longer than ten microseconds.

77. (Original) The integrated circuit of claim 65 wherein the programming voltage is within the range from 10 to 16 volts.

78. (Original) The integrated circuit of claim 65 wherein the substrate comprises a monocrystalline substrate including circuitry which is coupled to the memory array.

79. (Original) The integrated circuit of claim 78 wherein NAND strings of a given memory plane include selection devices formed above the substrate.

80. (Original) The integrated circuit of claim 65 wherein the substrate comprises a polycrystalline substrate.

81. (Original) The integrated circuit of claim 65 wherein the substrate comprises an insulating substrate.

82. (Original) The integrated circuit of claim 46 wherein the modifiable conductance switch devices comprise transistors having a depletion mode threshold voltage at least some of the time.

83. (Original) The integrated circuit of claim 46 including modifiable conductance switch devices chosen from the group consisting of:

a device including a floating gate electrode;

a device including silicon nanoparticles;

a device including a polarizable material; and

a device including a ferroelectric material.

84. **(Currently amended)** The integrated circuit of claim 51 ~~claim 46~~ wherein the modifiable conductance switch devices comprise thin film transistor (TFT) devices.

85. **(Currently amended)** The integrated circuit of claim 46 wherein the ~~memory cell~~ modifiable conductance switch devices have more than two nominal values of conductance, for storing more than one bit of data per memory cell.

86. **(Currently amended)** ~~The integrated circuit of claim 46~~ An integrated circuit comprising:

a memory array including memory cells arranged in a plurality of series-connected NAND strings, said memory cells comprising modifiable conductance switch devices; and

array support circuitry configured for pulsing a selected word line to a programming voltage a number of times to achieve an aggregate programming time for a selected memory cell, while limiting individual programming pulses to durations substantially less than the aggregate programming time, thereby limiting leakage current effects within NAND strings of a selected block;

wherein the modifiable conductance switch devices comprise transistors having a charge storage dielectric.

87. (Original) The integrated circuit of claim 86 wherein the charge storage dielectric comprises an oxide-nitride-oxide (ONO) stack.

88. **(Currently amended)** The integrated circuit of claim 86 wherein the ~~memory cell~~ transistors have a depletion mode threshold voltage for at least one of two data states.